IN THE SPECIFICATION

Please amend the Title on page 1, line 1, as follows:

~~Data Processing Apparatus and Data Processing Method~~

DATA PROCESSING APPARATUS AND METHOD FOR STAGED PIPELINE PROCESSING

Please amend the paragraph on page 2, lines 6-15, as follows:

Fig. 3 is a block diagram showing an example in which a plurality of pipeline processing portions are disposed inside the processor. An instruction read from an instruction cache (IC) 21 of Fig. 3 is dispatched to an empty pipeline processing portion among six pipeline processing portions (ALU) 24 via an instruction register (IR) 22, and then is executed by the empty pipeline processing portion. Data read out from a register file (RF) 23 in accordance with the instruction is calculated by the pipeline processing portion 24, and the execution result of the instruction is written back to a register file (RF) [[23]] 25.

Please amend the paragraph on page 10, lines 14-18, as follows:

On the other hand, Fig. 10 is a block diagram showing ~~a~~ an internal constitution ~~in~~ of the processor. The data is directly supplied to the first pipeline processing portion 1 from an instruction cache 31 via an instruction register 32, and once latched by the flip-flop 3 before supplied to the second pipeline processing portion 2.

Please amend the abstract on page 17, lines 3-19, as follows:

~~There is disclosed a~~ A data processing apparatus ~~which can reduce~~ that reduces a fanout load of a control signal for controlling a pipeline~~. The data processing apparatus of the present invention~~ includes a first pipeline processing portion for executing a processing in five divided stages, a second pipeline processing portion for executing a processing one stage behind the first pipeline processing portion, and a plurality of flip-flops for latching the control signals inputted to the respective stages. The second pipeline processing portion performs the processing in each stage based on delayed control signals ~~Control A to E~~ generated by once latching the control signals ~~Control A to E~~ inputted to the respective stages by the flip-flop~~. Because of this~~, thereby reducing the fanout load and signal delay of the control signals ~~Control A to E is reduced, and signal delay of the control signals Control A to E can be reduced~~. Moreover, a wiring length of a control line for transmitting the control signals ~~Control A to E~~ can be set to be longer than a conventional wiring length.